

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**Patent Application**

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Applicant(s): Bapst et al.  
Docket No.: YOR920030633US1  
Serial No.: 10/775,854  
Filing Date: February 10, 2004  
10 Group: 2883  
Examiner: Jerry M. Blevins

Title: Circuit Board Integrated Optical Coupling Elements

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**COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE**

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Mail Stop Issue Fee  
Commissioner for Patents  
P O. Box 1450  
Alexandria, VA 22313-1450

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Sir:

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The following remarks are submitted in response to the Examiner's Statement of Reasons for Allowance included in the Notice of Allowability dated December 26, 2006 in the above-identified application.

COMMENTS

Applicants note that, in the Statement of Reasons for Allowability, the Examiner alleges that Gallup teaches using the one or more etch stop layers to selectively remove material to provide one or more cavities having a defined position and depth,  
5 wherein the one or more cavities provide for an optical alignment of one or more optical elements.

As argued in the Memorandum in Support of Pre-Appeal Brief Request for Review dated November 14, 2006, Applicants maintain that Gallup does not disclose or suggest using one or more etch stop layers and providing one or more cavities having a  
10 defined positioning and depth in the circuit board, wherein said one or more cavities provide for an alignment of one or more optical elements, as required by independent claims 1 and 21.

The Examiner's attention to this matter is appreciated.

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Respectfully submitted,

*Kevin M. Mason*

Date: March 15, 2007  
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